Serial No.: 10/629,041

Group Art Unit: 2818

REMARKS

The Examiner indicated this application is in condition for allowance except for the

following formal matters:

A. The title of the invention is not descriptive.

Applicants have amended the Title to "METHOD USING QUASI-PLANAR

DOUBLE GATED FIN FIELD EFFECT TRANSISTOR PROCESS FOR THE

FABRICATION OF A THYRISTOR-BASED STATIC READ/WRITE RANDOM-ACCESS

MEMORY" to clearly indicate the invention to which the allowed method claims are

directed.

B. Cancellation of non-elective device claims 11-20.

Applicants have canceled claims 11-20, but reserve the right to file a divisional patent

application related thereto.

C. In Title, it is requested that Applicants spell out the acronym so as to avoid any

possible confusion as to the meaning.

Applicants have replaced the acronym FINFET in the title with "Fin Field Effect

Transistor". In addition, the acronym SRAM has been replaced with "Static Read/Write

Random-Access Memory".

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance.

Allowance of claims 1-10 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is

hereby made. Please charge any shortage in fees due in connection with the filing of this

paper, including any extension of time fees, to Deposit Account No. 50-0374 and please

credit any excess fees to such deposit account.

Respectfully submitted,

Wikis Schinam

Mikio Ishimaru

Registration No. 27,449

The Law Offices of Mikio Ishimaru

Telephone: (408) 738-0592

Date: November 26, 2004

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